

(19) World Intellectual Property Organization
International Bureau



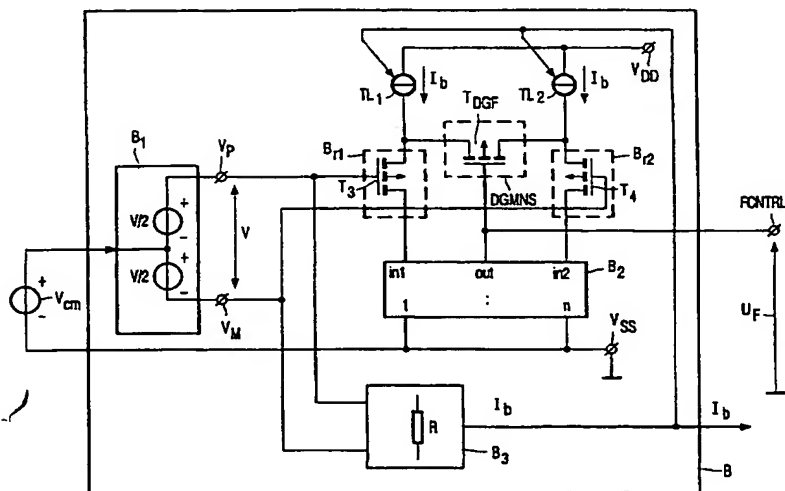
(43) International Publication Date
30 August 2001 (30.08.2001)

PCT

(10) International Publication Number
WO 01/63754 A1

- (51) International Patent Classification⁷: H03F 3/45 (74) Agent: DUIJVESTIJN, Adrianus, J.; Internationaal Octrooibureau B.V., Prof Holstlaan 6, NL-5656 AA Eindhoven (NL).
- (21) International Application Number: PCT/EP01/01231
- (22) International Filing Date: 5 February 2001 (05.02.2001) (81) Designated States (*national*): JP, KR.
- (25) Filing Language: English (84) Designated States (*regional*): European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR).
- (26) Publication Language: English
- (30) Priority Data: 00200636.9 24 February 2000 (24.02.2000) EP Published:
— with international search report
- (71) Applicant: KONINKLIJKE PHILIPS ELECTRONICS N.V. [NL/NL]; Groenewoudseweg 1, NL-5621 BA Eindhoven (NL). For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.
- (72) Inventor: BLANKEN, Pieter, G.; Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL).

(54) Title: ELECTRONIC CIRCUIT COMPRISING A DIFFERENTIAL PAIR PROVIDED WITH DEGENERATION MEANS FOR DEGENERATING A TRANSCONDUCTANCE OF THE DIFFERENTIAL PAIR



(57) Abstract: An electronic circuit comprising a differential pair (T_1 , T_2) provided with degeneration means (DGMNS) for degenerating a transconductance of the differential pair (T_1 , T_2), and an auxiliary circuit (B) for supplying a control voltage (U) to a control terminal (CNTRL) of the degeneration means (DGMNS). The auxiliary circuit (B) also accomplishes a DC-biasing of the differential pair (T_1 , T_2). Said control voltage (U) and the DC-biasing are such that the transconductance of the differential pair (T_1 , T_2) is virtually independent of the value of the control voltage (U) and virtually independent of the DC-biasing of the differential pair (T_1 , T_2). The auxiliary circuit (B) comprises a further differential pair (T_3 , T_4) provided with further degeneration means (FDGMNS) for degenerating a transconductance of

the further differential pair (T_3 , T_4). The auxiliary circuit (B) is arranged for supplying a further control voltage (U_F) to a control terminal (FCNTRL) of the further degeneration means (FDGMNS). The control voltage (U) is dependent on the further control voltage (U_F). The further control voltage (U_F) and the control voltage (U) can, for instance, be the same voltage. The auxiliary circuit (B) comprises means (B_2) for generating a desired current ratio (n) between a first branch (B_{r1}) and a second branch (B_{r2}) of the further differential pair (T_3 , T_4). The auxiliary circuit (B) comprises means (B_1) for generating a first DC-voltage (V_P) to a first input terminal of the further differential pair (T_3 , T_4), and a second DC-voltage (V_M) to a second input terminal of the further differential pair (T_3 , T_4).

WO 01/63754 A1

Electronic circuit comprising a differential pair provided with degeneration means for degenerating a transconductance of the differential pair

The invention relates to an electronic circuit comprising a differential pair which is provided with degeneration means for degenerating a transconductance of the differential pair, and an auxiliary circuit for providing a control voltage to a control electrode of the degeneration means.

- 5 Such an electronic circuit is known from US patent US 5,642,078. The known circuit is shown in Fig. 1 and comprises inter alia a differential pair consisting of a field effect transistor 22 and a field effect transistor 23. The differential pair further comprises a field effect transistor 16 which is connected by a source to the source of the field effect transistor 23 and which is connected by a drain to the source of the field effect transistor 22.
- 10 The gate of the field effect transistor 16 is connected to a bias control circuit. The required direct currents for the differential pair are supplied by a current source 20 and a current source 21. The field effect transistor 16 is set for its linear operation range and serves to degenerate the transconductance of the differential pair.

- 15 It is a disadvantage of the known electronic circuit that the transconductance of the differential pair is not accurately defined.

It is an object of the invention to provide an electronic circuit comprising a differential pair whose transconductance is accurately defined.

- 20 According to the invention, the electronic circuit mentioned in the opening paragraph is for this purpose characterized in that the auxiliary circuit is designed for providing a DC biasing of the differential pair, and in that the auxiliary circuit is designed such that the transconductance of the differential pair is substantially independent of the value of the control voltage and of the DC biasing of the differential pair.

- 25 Since not only the control voltage at the control electrode of the degeneration means is regulated, as in the known circuit, but also the DC currents of the differential pair are regulated, it can be achieved that the transconductance of the differential pair becomes equal to a desired reference value. The reference value may be obtained, for example, through the use of a reference resistance. The reference resistance may be obtained in various alternative ways, for example through the use of a ratio of resistance values, a capacitor, a

ratio of capacitance values, a voltage source, a ratio of voltage values, a current source, a ratio of current values, etc.

An embodiment of an electronic circuit according to the invention is characterized in that the auxiliary circuit comprises a further differential pair comprising
5 further degeneration means for degenerating a transconductance of said further differential pair, and in that the auxiliary circuit is furthermore designed for providing a further control voltage to a control electrode of the further degeneration means, and in that the control voltage is dependent on said further control voltage.

10 An electronic circuit according to the invention is implemented thereby in a simple manner. If so desired, the degeneration means and the further degeneration means may be constructed in a similar manner. It is also possible to choose the control voltage to be equal to the further control voltage.

An embodiment of an electronic circuit according to the invention is characterized in that the auxiliary circuit comprises current bias means for providing a
15 desired current ratio between a first current branch and a second current branch of the further differential pair.

This renders it simpler to obtain a correct DC biasing of the differential pair.

An embodiment of an electronic circuit according to the invention is characterized in that the current bias means are provided with a first input which is coupled to
20 the first current branch, a second input which is coupled to the second current branch, and an output which is coupled to the control electrode of the further degeneration means.

The current bias means control the control electrode of the further degeneration means such that the ratio of the respective currents of the first and the second current branch is equal to the desired current ratio.

25 An embodiment of an electronic circuit according to the invention is characterized in that the auxiliary circuit furthermore comprises voltage bias means for providing a first bias voltage to a first input of the further differential pair and a second bias voltage to a second input of the further differential pair, and in that the further differential pair further comprises first current supply means connected in series with the first current
30 branch and second current supply means connected in series with the second current branch, and in that the currents supplied by said first current supply means and second current supply means are dependent on the difference between the first bias voltage and the second bias voltage.

It is achieved thereby that not only the desired current ratio of the first and the second current branch is equal to the desired current ratio, but that also the absolute values of the currents through the first and the second current branch are defined.

5 An embodiment of an electronic circuit according to the invention is characterized in that said currents are approximately linearly dependent on the difference between the first bias voltage and the second bias voltage.

This renders it possible to generate said currents in a simple manner.

10 An embodiment of an electronic circuit according to the invention is characterized in that the degeneration means comprise a field effect transistor which is set for its linear operation range, and in that the further degeneration means comprise a further field effect transistor which is set for its linear operation range.

A further linearizing of the differential pair is realized thereby, so that the distortion of the differential pair is reduced.

15 An embodiment of an electronic circuit according to the invention is characterized in that the value of the first bias voltage corresponds to the highest value of the first bias voltage at which the electronic circuit can still function correctly, and in that the value of the second bias voltage corresponds to the lowest value of the second bias voltage at which the electronic circuit can still function correctly.

20 This has the advantage that the differential pair continues to function correctly also at the widest possible signal control range at the inputs of the differential pair.

A further advantageous embodiment of an electronic circuit according to the invention is defined in claim 10.

25 The invention will be explained in more detail below with reference to the accompanying drawing, in which:

Fig. 1 shows a known electronic circuit with a differential pair and a field effect transistor for degenerating the transconductance of the differential pair,

30 Fig. 2 is a circuit diagram of a differential pair which is known per se and which is provided with a field effect transistor for degenerating the transconductance of the differential pair, and which can serve as a basic circuit for realizing a differential pair according to the invention,

Fig. 3 is a circuit diagram of an auxiliary circuit designed for providing a DC biasing of a differential pair,

Fig. 4 is a circuit diagram of voltage bias means for providing a first and a second bias voltage to the inputs of the differential pair of the auxiliary circuit,

Fig. 5 shows an alternative circuit diagram of voltage bias means which supplies not only the first and the second bias voltage but also a common-mode voltage and a cascode voltage for the auxiliary circuit,

Fig. 6 shows a circuit diagram of an embodiment of the further differential pair,

Fig. 7 shows a circuit diagram of a current-generating circuit for supplying the current I_b ,

Fig. 8 shows a circuit diagram of a so-called g_m/C filter known from the state of the art,

Fig. 9 shows an electronic circuit comprising several differential pairs which are all controlled by an auxiliary circuit according to the invention, and

Fig. 10 shows a circuit diagram which is an alternative to the auxiliary circuit of Fig. 3.

The same components or elements have been given the same reference symbols in these Figures.

Fig. 2 shows an embodiment of a differential pair which is known per se. The differential pair comprises a first transistor T_1 , a second transistor T_2 , degeneration means DGMNS constructed with a field effect transistor T_{DG} , a current source I_1 , and a current source I_2 . The field effect transistor T_{DG} is connected with its source and drain between the sources of the transistors T_1 and T_2 . The gate of the field effect transistor T_{DG} is connected to a control electrode CNTRL for receiving a control voltage U between the control electrodes CNTRL and a supply terminal V_{SS} . The current source I_1 is connected between a further supply terminal V_{DD} and the source of the transistor T_1 . The current source I_2 is connected between the further supply terminal V_{DD} and the source of the transistor T_2 . The gate of the transistor T_1 is connected to a terminal 1 which is a first input of the differential pair. The gate of the transistor T_2 is connected to a terminal 2 which is a second input of the differential pair. The drain of the first transistor T_1 is connected to a terminal 3 which is a first output of the differential pair. The drain of the transistor T_2 is connected to a terminal 4 which is a second output of the differential pair. The values of the currents supplied by the first and the second current source I_1 and I_2 are referenced I_b . The field effect transistor T_{DG} is set for its linear operation range, so that it behaves approximately as a linear resistance whose value

can be varied by means of the control voltage U. The control voltage U and the currents I_b are supplied from the auxiliary circuit B according to the invention shown in Fig. 3.

Fig. 3 shows the circuit diagram of the auxiliary circuit B. The auxiliary circuit B comprises a further differential pair which is composed in a similar manner as the differential pair of Fig. 2. Transistors T_3 and T_4 correspond to the transistors T_1 and T_2 , respectively. A further field effect transistor T_{DGF} corresponds to the field effect transistor T_{DG} . Current sources TL_1 and TL_2 correspond to the current sources I_1 and I_2 , respectively.

The auxiliary circuit B further comprises voltage bias means B_1 , current bias means B_2 , and a current-generating circuit B_3 . A common-mode voltage V_{cm} is supplied to the voltage bias means B_1 . The voltage bias means B_1 supply a first bias voltage V_p to the gate of the transistor T_3 and a second bias voltage V_M to the gate of the transistor T_4 . The difference between the first bias voltage V_p and the second bias voltage V_M is indicated with V. The first bias voltage V_p is equal to the common-mode voltage V_{cm} plus half the differential voltage V. The second bias voltage V_M is equal to the common-mode voltage V_{cm} minus half the differential voltage V. The current-generating circuit B_3 is connected so as to receive the differential voltage V and supplies the currents I_b to the further differential pair of the auxiliary circuit B and to the differential pair of Fig. 2. The current bias means B_2 are provided with a first input in1 which is connected to the drain of the transistor T_3 , a second input in2 which is connected to the drain of the transistor T_4 , and an output out which is connected to the gate of the further field effect transistor T_{DGF} and to the further control electrode FCNTRL for supplying a further control voltage U_F .

The circuit operates as follows. The value of the currents I_b supplied by the current-generating circuit B_3 can be calculated from equation 1:

$$I_b = m \cdot \frac{V}{R} \quad (1)$$

in which: R is the value of a reference resistance, and m is a scaling value.

The current bias means B_2 supply the currents through the transistor T_3 and the transistor T_4 such that they have a ratio of 1:n through modification of the further control voltage U_F at the gate of the further field effect transistor T_{DGF} . Since the current ratio of the transistors T_3 and T_4 is controlled by the current bias means B_2 , and since the currents supplied by the current sources TL_1 and TL_2 are also controlled by the current-generating circuit B_3 , the transconductance g_m of a differential pair controlled by the auxiliary circuit B is defined by equation 2:

$$g_m = \frac{1}{R} \cdot \frac{n-1}{n+1} \cdot m \quad (2)$$

The scaling factor m is preferably independent of the temperature and independent of process parameters. This may be realized in a simple manner through standard IC design techniques. The reference value R may be accurately defined in a simple manner, for example through the use of a discrete resistor. It follows from equation 2 that the transconductance g_m of a differential pair is accurately defined then.

Fig. 4 is a circuit diagram of a first embodiment of the voltage bias means B_1 . The voltage bias means B_1 comprise transistors T_5 to T_8 , a diode D , a current source I_3 , and a voltage source V_{cas} . The sources of the transistors T_5 and T_7 are connected to the further supply terminal V_{DD} . The drains of the transistors T_5 and T_7 are interconnected, as are the sources of the transistors T_6 and T_8 . The drain of the transistor T_6 is connected to the gate of the transistor T_5 , to a terminal V_p , and to a first electrode of the diode D . The drain of the transistor T_8 is connected to the gate of the transistor T_7 , to a terminal V_M , and to a second electrode of the diode D . The current source I_3 is connected between the terminal V_M and the supply terminal V_{SS} . The voltage source V_{cas} is connected between the gate of the transistor T_6 and the further supply terminal V_{DD} .

The transistors T_6 and T_8 are connected as a differential pair. Since the gates of the transistors T_6 and T_8 are interconnected, and the sources of the transistors T_6 and T_8 are interconnected, the transistors T_6 and T_8 pass equal currents. The current supplied by the current source I_3 has a value $2I_b$, so the currents running through the transistors T_6 and T_8 are equal to I_b . (Since the gate-source voltages of the transistors T_5 and T_7 are different, the currents through the transistors T_5 and T_7 are different, but the sum of the currents through the transistors T_5 and T_7 is equal to $2I_b$.) So the current flowing through the diode D is equal to I_b . The voltage drop across the diode D is equal to the differential voltage V . Since the gates of the transistors T_5 and T_7 are coupled to the terminals V_p and V_M , respectively, the voltages V_p and V_M are defined. The diode D may be replaced by an alternative element across which a voltage drop can be generated such as, for example, a resistor.

Fig. 5 shows a circuit diagram of a second embodiment of the voltage bias means B_1 . The circuit comprises transistors T_5 , T_6 , T_9 , and T_{10} . The circuit further comprises the diode D , resistors R_1 and R_2 , and current sources I_4 and I_5 . The sources of the transistors T_5 and T_9 are connected to the further supply terminal V_{DD} . The sources of the transistors T_6 and T_{10} are connected to the drain of the transistor T_5 and the drain of the transistor T_9 ,

respectively. The gates of the transistors T_6 and T_{10} and the drain of the transistor T_{10} are interconnected. The gate of the transistor T_5 is connected to the drain of the transistor T_6 , to the terminal V_p , to the first electrode of the diode D , and to a first electrode of the resistor R_1 . The second electrode of the resistor R_1 is connected to a first electrode of the resistor R_2 and to the gate of the transistor T_9 . The second electrode of the diode D is connected to a second electrode of the resistor R_2 and to the terminal V_M . The current source I_4 is connected between the terminal V_M and the supply terminal V_{SS} . The current source I_5 is connected between the drain of the transistor T_{10} and the supply terminal V_{SS} . The voltage source V_{cas} required in Fig. 4 is not necessary in the circuit of Fig. 5 because the voltage V_{cas} is generated by the circuit itself. A further advantage of the circuit of Fig. 5 is that it supplies the required common-mode voltage V_{cm} (see Fig. 3). Again, the diode D may be replaced by an alternative element in this circuit. It is also possible, however, to leave out the diode D and not replace it with another element. The function of the diode D is taken over in that case by the series arrangement of the resistors R_1 and R_2 .

It should be noted that it may be necessary in the case of a differential pair as shown, for example, in Fig. 2, that there is a common mode voltage control at the inputs thereof. The manner in which this is realized is generally known. A circuit may be used for this, for example, such as the arrangement of transistors T_5 , T_6 , T_7 , T_8 and the voltage source V_{cas} as shown in Fig. 4. To define the transconductance g_m of a differential pair as accurately as possible (so that no significant deviation arises from the calculated transconductance in accordance with equation 2), it is advisable to choose the DC voltages at terminals 1 and 2 (see Fig. 2) to be equal as much as possible to the DC voltages of the first bias voltage V_p and the second bias voltage V_M , respectively (see Fig. 3).

Fig. 6 shows the circuit diagram of an embodiment of the further differential pair. The difference with the further differential pair as shown in Fig. 3 is that the current bias means B_2 are constructed with a current mirror CM. The input in1 of the current mirror CM is connected to the drain of the transistor T_3 . The output out of the current mirror CM is connected to the drain of the transistor T_4 and to the gate of the further field effect transistor T_{DGF} . The further differential pair may alternatively be constructed with other types of differential pairs, for example cascoded differential pairs. The current mirror CM may simply be composed from two transistors in accordance with the state of the art. More complicated types of current mirrors may also be used, for example cascoded current mirrors.

Fig. 7 is a circuit diagram of an embodiment of a current-generating circuit B_4 for supplying the currents I_b . The circuit comprises transistors T_{11} to T_{17} , a resistor R_3 , and a diode D_2 . The sources of the transistors T_{13} to T_{17} are connected to the supply terminal V_{SS} .

The gates of the transistors T_{13} to T_{17} are interconnected. The drain of the transistor T_{14} is connected to the gate of the transistor T_{14} and to the drain of the transistor T_{12} . The resistor R_3 is connected between the source of the transistor T_{12} and the further supply terminal V_{DD} . The drain of the transistor T_{13} , the drain of the transistor T_{11} , and the gates of the transistors T_{11} and T_{12} are interconnected. The diode D_2 is connected between the source of the transistor T_{11} and the further supply terminal V_{DD} . The drains of the transistors T_{15} to T_{17} supply the desired currents I_b . It should be noted that the current-generating circuit B_4 may be provided with a start circuit in accordance with the state of the art for preventing starting problems.

The current-generating circuit B_4 of Fig. 7 will now be explained in more detail in combination with Fig. 10. In Fig. 10, the current-generating circuit B_3 of Fig. 3 is replaced by a current-generating circuit B_4 . The differential voltage V between the terminals V_P and V_M is not supplied to the current-generating circuit B_4 in the auxiliary circuit of Fig. 10. A further difference with Fig. 3 is that a current I_b is supplied to the voltage bias means B_1 . So the current $2I_b$ supplied by the current source I_3 in Fig. 4 is supplied from the current-generating circuit B_4 or, if the voltage bias means B_1 are constructed in accordance with Fig. 5, the currents I_b supplied by the current sources I_4 and I_5 are supplied from the current-generating circuit B_4 here. Now if the diode D_2 of Fig. 7 is constructed so as to be identical to the diode D of Fig. 4 or Fig. 5, the voltage V across the diode D_2 will be substantially equal to the differential voltage V of Fig. 3 or Fig. 10. The voltage V across the diode D_2 of Fig. 7 accordingly is not directly a result of the voltage V of Fig. 3 or Fig. 10, but is generated by the current-generating circuit B_4 . This renders it possible for an electrode of the diode D_2 to be at a fixed potential. In the present case, the anode of the diode D_2 is connected to the further supply terminal V_{DD} . This renders it easier to realize the current-generating circuit B_4 as compared with the current-generating circuit B_3 . Fig. 7 shows that three currents I_b are supplied from the drains of the transistors T_{15} to T_{17} . This is merely an example, the desired number of currents I_b may be adapted in a simple manner. Suppose, for example, that the auxiliary circuit B of Fig. 10 is used, and that three differential pairs as shown in Fig. 2 are controlled by means of the further control signal U_F , and that the circuit of Fig. 5 is used for the voltage bias means B_1 . Each differential pair requires two currents I_b . The further differential pair also requires two currents I_b . The voltage bias means B_1 also require two currents I_b . The number of currents I_b to be supplied by the current-generating circuit B_4 in this example is equal to 10. It should be noted that the currents I_b (in this example) cannot be derived directly from the current-generating circuit B_4 for the differential pairs and the

further differential pair. This is because these currents are to be reversed in direction first, for example by means of a current mirror.

Fig. 8 is a circuit diagram of a g_m/C filter which is known per se. In this example, the g_m/C filter comprises three differential pairs DF_1 , DF_2 , and DF_3 , which may be constructed, for example, as shown in the circuit diagram of Fig. 2. The outputs of the differential pairs DF_1 to DF_3 are coupled to respective capacitors C_1 to C_3 . The g_m/C filter further comprises a building block TS. The building block TS supplies control signals U_1 to U_3 to the gates of the degeneration field effect transistors of the differential pairs DF_1 to DF_3 . Such g_m/C filters are used, for example, in so-called sigma-delta AD converters.

A disadvantage of known g_m/C filters is that the transconductance of the differential pairs DF_1 to DF_3 is not accurately defined. This may lead to a wide spread in the zero points with the use in a sigma-delta AD converter.

This disadvantage is eliminated in that the differential pairs DF_1 to DF_3 are controlled by the auxiliary circuit B according to the invention as shown in Fig. 9. The gates of all degeneration field effect transistors are controlled here with the same control voltage U . Moreover, each differential pair DF_1 to DF_3 receives the same current I_b . Starting from the assumption that the differential pairs DF_1 to DF_3 are of the same construction, the transconductance values of said differential pairs will be the same. If it should be desirable to obtain twice the transconductance for the differential pair DF_2 only, for example, a simple solution is to connect two differential pairs in parallel. The circuit of Fig. 9 may be used, for example, for realizing an improved g_m/C filter. The differential pairs DF_1 to DF_3 are coupled to one another in the same manner as in Fig. 8, and capacitors C_1 to C_3 are also added in the same manner.

The electronic circuit may be implemented both with discrete components and in the form of an integrated circuit. Except for the degeneration field effect transistors, the other field effect transistors may be replaced with bipolar transistors. It is also possible to replace all p-conductivity type transistors with n-conductivity type transistors provided all n-conductivity type transistors are replaced with p-conductivity type transistors at the same time.

CLAIMS:

1. An electronic circuit comprising a differential pair (T_1 , T_2) which is provided with degeneration means (DGMNS) for degenerating a transconductance of the differential pair (T_1 , T_2), and an auxiliary circuit (B) for providing a control voltage (U) to a control electrode (CNTRL) of the degeneration means (DGMNS), characterized in that the auxiliary
5 circuit (B) is designed for providing a DC biasing of the differential pair (T_1 , T_2), and in that the auxiliary circuit (B) is designed such that the transconductance of the differential pair (T_1 , T_2) is substantially independent of the value of the control voltage (U) and of the DC biasing of the differential pair (T_1 , T_2).
- 10 2. An electronic circuit as claimed in claim 1, characterized in that the auxiliary circuit (B) comprises a further differential pair (T_3 , T_4) comprising further degeneration means (FDGMNS) for degenerating a transconductance of said further differential pair (T_3 , T_4), and in that the auxiliary circuit (B) is furthermore designed for providing a further
15 control voltage (U_F) to a control electrode (FCNTRL) of the further degeneration means (FDGMNS), and in that the control voltage (U) is dependent on said further control voltage (U_F).
3. An electronic circuit as claimed in claim 2, characterized in that the auxiliary
20 circuit (B) comprises current bias means (B_2) for providing a desired current ratio (n) between a first current branch (Br_1) and a second current branch (Br_2) of the further differential pair (T_3 , T_4).
4. An electronic circuit as claimed in claim 3, characterized in that the current
25 bias means (B_2) are provided with a first input (in1) which is coupled to the first current branch (Br_1), a second input (in2) which is coupled to the second current branch (Br_2), and an output (out) which is coupled to the control electrode (FCNTRL) of the further degeneration means FDGMNS).
5. An electronic circuit as claimed in claim 4, characterized in that the auxiliary
30 circuit (B) furthermore comprises voltage bias means (B_1) for providing a first bias voltage

(V_P) to a first input of the further differential pair (T_3 , T_4) and a second bias voltage (V_M) to a second input of the further differential pair (T_3 , T_4), and in that the further differential pair (T_3 , T_4) further comprises first current supply means (TL_1) connected in series with the first current branch (Br_1) and second current supply means (TL_2) connected in series with the second current branch (Br_2), and in that the currents supplied by said first current supply means (TL_1) and second current supply means (TL_2) are dependent on the difference (V) between the first bias voltage (V_P) and the second bias voltage (V_M).

6. An electronic circuit as claimed in claim 5, characterized in that said currents are approximately linearly dependent on the difference (V) between the first bias voltage (V_P) and the second bias voltage (V_M).

7. An electronic circuit as claimed in claims 1, 2, 3, 4, 5, or 6, characterized in that the degeneration means (DGMNS) comprise a field effect transistor (T_{DG}) which is set for its linear operation range, and in that the further degeneration means (FDGMNS) comprise a further field effect transistor (T_{DGF}) which is set for its linear operation range.

8. An electronic circuit as claimed in claim 2, 3, 4, 5, 6, or 7, characterized in that the value of the control voltage (U) is approximately equal to the value of the further control voltage (U_F).

9. An electronic circuit as claimed in claim 5, 6, 7, or 8 in as far as it is dependent on claim 5, characterized in that the value of the first bias voltage (V_P) corresponds to the highest value of the first bias voltage (V_P) at which the electronic circuit can still function correctly, and in that the value of the second bias voltage (V_M) corresponds to the lowest value of the second bias voltage (V_M) at which the electronic circuit can still function correctly.

10. An electronic circuit as claimed in claim 3, characterized in that the current bias means (B_2) comprise a current mirror (CM) which is provided with an input (in1) coupled to the first current branch (Br_1) and an output (out) coupled to the second current branch (Br_2), said output (out) being coupled to the control electrode (FCNTRL) of the further degeneration means (FDGMNS).

2/6

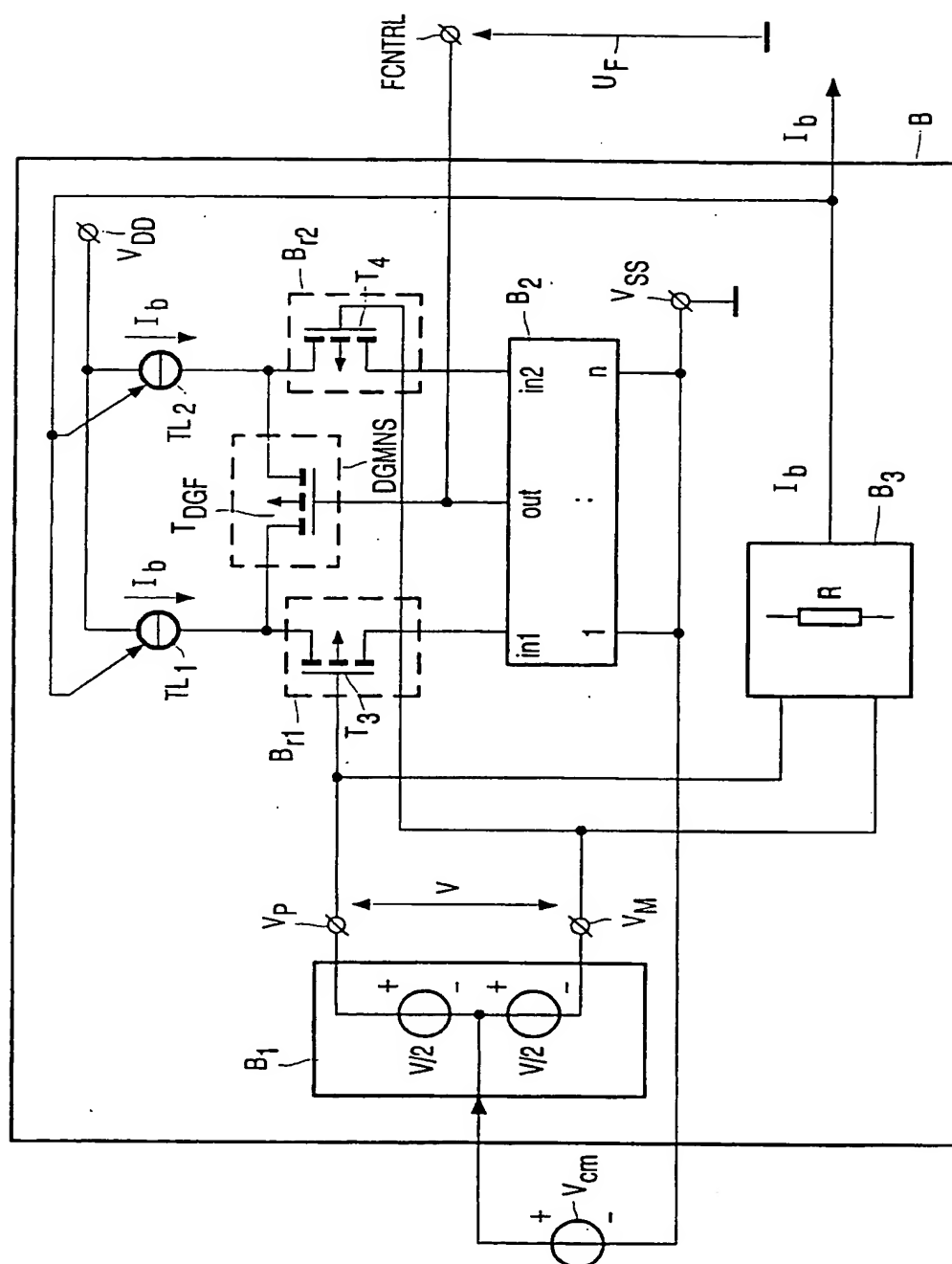


FIG. 3

3/6

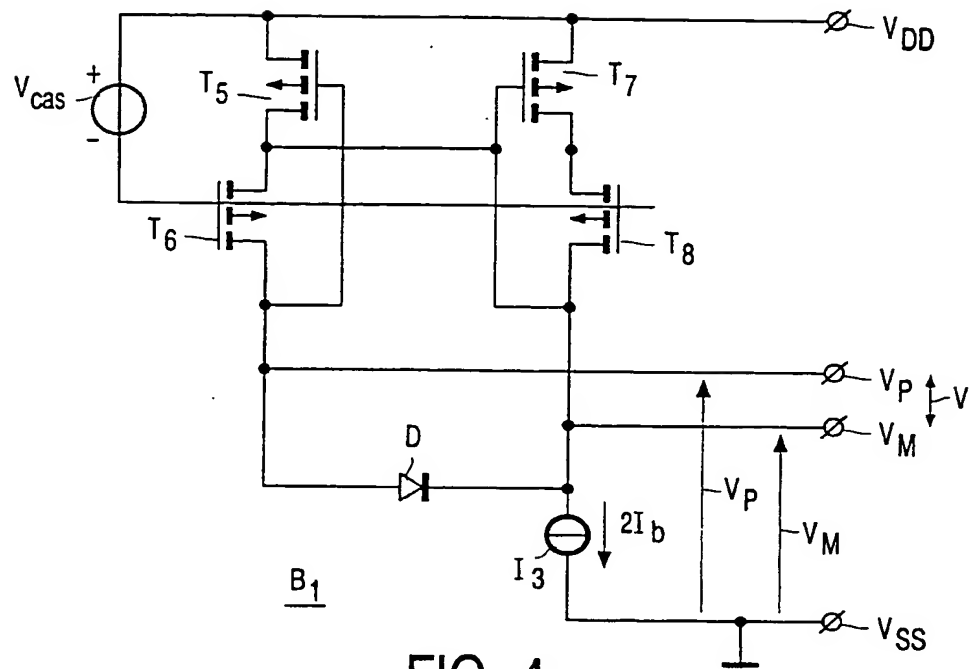


FIG. 4

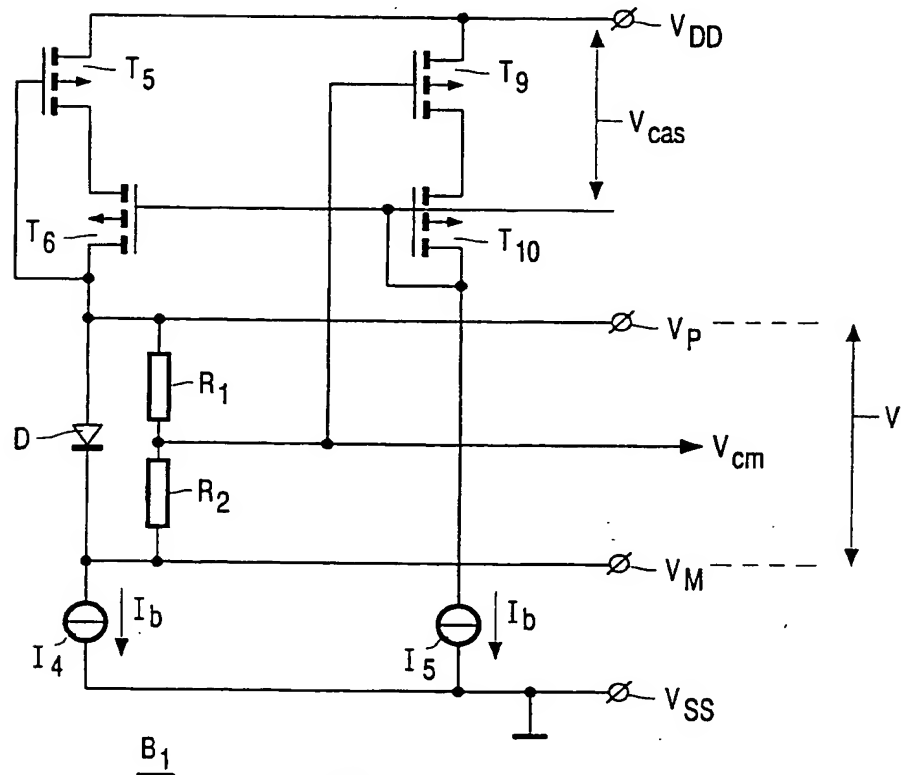


FIG. 5

5/6

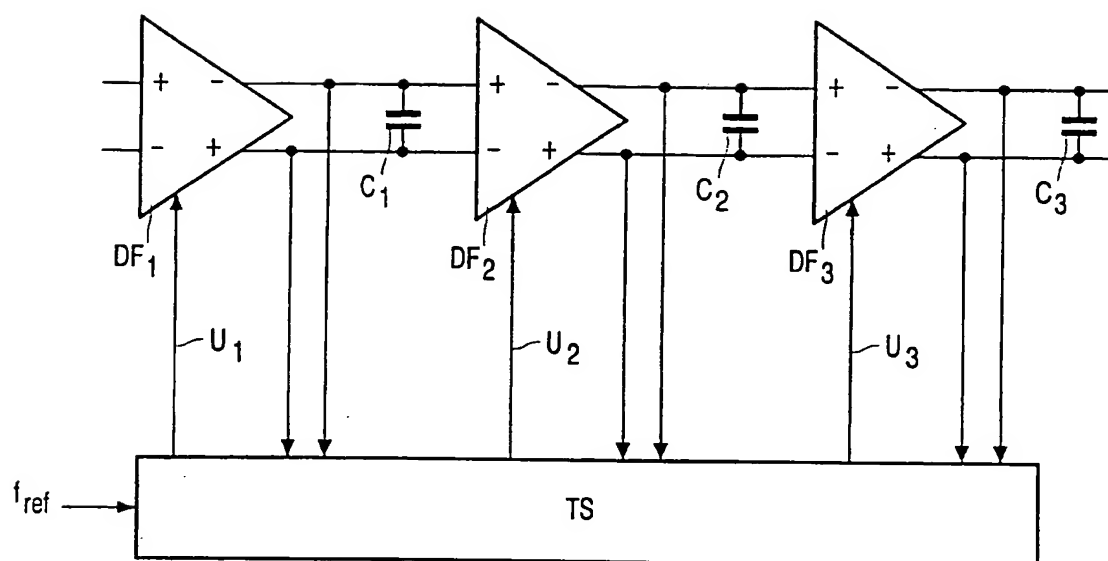


FIG. 8

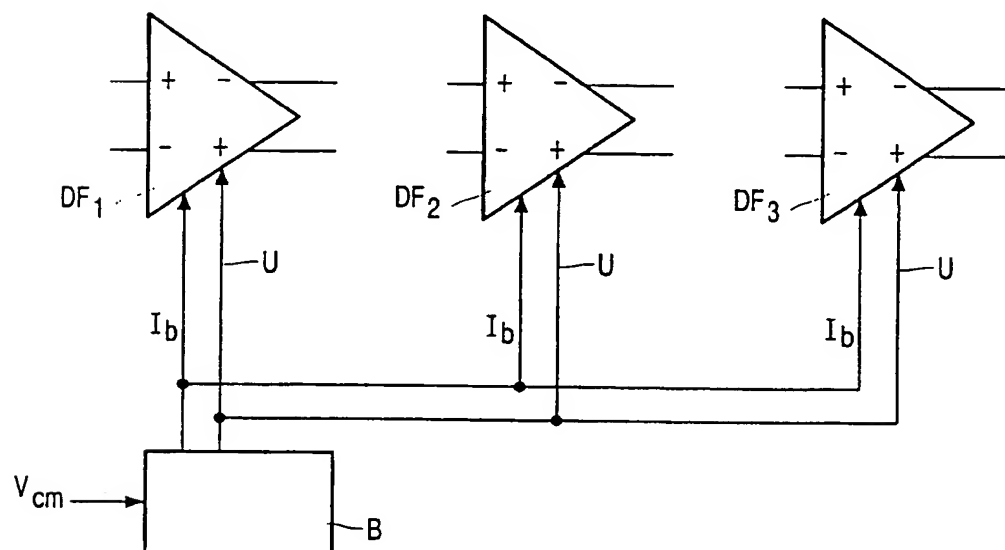


FIG. 9

6/6

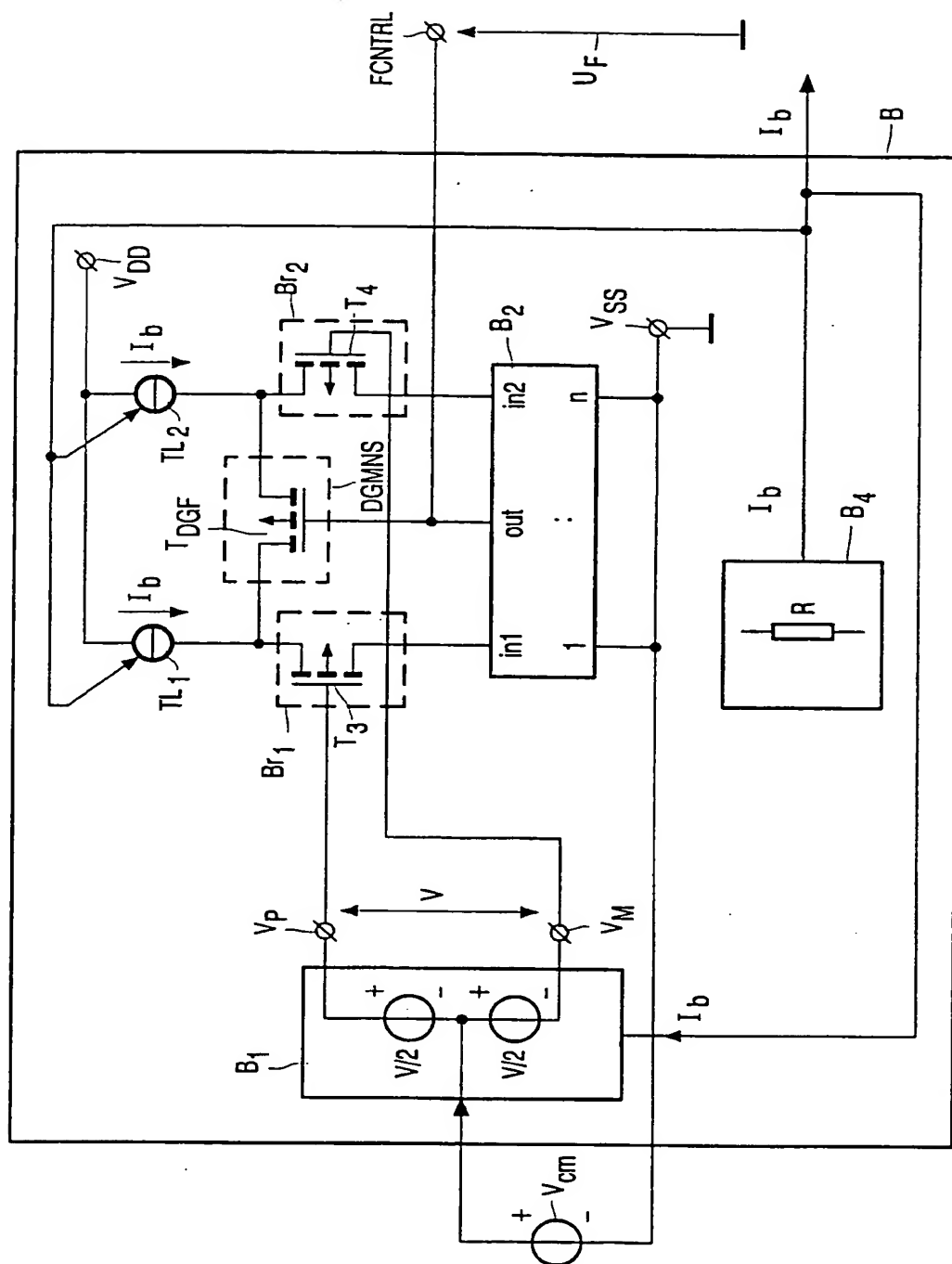


FIG. 10

INTERNATIONAL SEARCH REPORT

International Application No
PCT/EP 01/01231

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H03F3/45

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H03F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5 642 078 A (NAVABI MOHAMMAD J ET AL) 24 June 1997 (1997-06-24) cited in the application column 4, line 15 -column 5, line 57; figures 1,2,6	1
Y	US 4 388 539 A (BOEKE WOUTER M) 14 June 1983 (1983-06-14)	1
A	the whole document	2-10
A	WO 96 31945 A (PHILIPS ELECTRONICS NV ;PHILIPS NORDEN AB (SE)) 10 October 1996 (1996-10-10) abstract; figure 1	2,7
	-/--	

☒ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

* Special categories of cited documents :

- *A* document defining the general state of the art which is not considered to be of particular relevance
- *E* earlier document but published on or after the international filing date
- *L* document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
- *O* document referring to an oral disclosure, use, exhibition or other means
- *P* document published prior to the international filing date but later than the priority date claimed

- *T* later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
- *X* document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
- *Y* document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.
- *Z* document member of the same patent family

Date of the actual completion of the international search

30 March 2001

Date of mailing of the international search report

05/04/2001

Name and mailing address of the ISA

European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
Tel. (+31-70) 340-2040, Tx. 31 651 epo nl,
Fax: (+31-70) 340-3016

Authorized officer

Tyberghien, G

BEST AVAILABLE COPY

INTERNATIONAL SEARCH REPORT

International Application No

PCT/EP 01/01231

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	<p>US 6 011 437 A (JUSUF GANI ET AL) 4 January 2000 (2000-01-04) column 2, line 56 -column 5, line 15; figures 2A-3</p> <p>-----</p>	1-10

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No

PCT/EP 01/01231

Patent document cited in search report		Publication date	Patent family member(s)	Publication date
US 5642078	A	24-06-1997	NONE	
US 4388539	A	14-06-1983	NL 8001115 A	16-09-1981
			AU 539887 B	18-10-1984
			AU 6757781 A	03-09-1981
			BE 887643 A	24-08-1981
			CA 1165826 A	17-04-1984
			DE 3106558 A	07-01-1982
			FR 2476940 A	28-08-1981
			GB 2070360 A, B	03-09-1981
			HK 75584 A	12-10-1984
			JP 1004364 B	25-01-1989
			JP 1526010 C	30-10-1989
			JP 56168298 A	24-12-1981
			SE 450676 B	13-07-1987
			SE 8101161 A	26-08-1981
WO 9631945	A	10-10-1996	DE 69609272 D	17-08-2000
			DE 69609272 T	15-03-2001
			EP 0764364 A	26-03-1997
			JP 10501672 T	10-02-1998
			US 5668502 A	16-09-1997
US 6011437	A	04-01-2000	NONE	

BEST AVAILABLE COPY